X-CMOS 0.6

0.6 Micron
Modular Mixed Signal Technology [XC06]

Description

The XC06 Series completes X-FAB's 0.6 Micron Modular Mixed Signal Technology with embedded Non Volatile Memory and High Voltage options. EEPROM blocks up to 32 kbit as well as Flash memories up to 512 kbit can be integrated in standard cell, semi-custom and full custom designs for Industrial, Automotive and Telecommunication products.

MOS as well as Bipolar Transistors are available with Breakdown Voltages up to 100V.

The 5 V CMOS core is compatible in Design Rules and Transistor Performance with state of the art 0.6 µm CMOS Processes.

For Analog Application several capacitor and resistor devices are realized, using the Double-Poly-Non-Volatile-Memory architecture.

Reliable design rules, precise SPICE models, analog and digital libraries, IP's and development kits support the process for major CAE vendors.

Key Features

- 0.6-micron single poly, double metal N-well CMOS basic process
- Triple metal option for high density circuits
- Different medium and high voltage options with 8 to 40 V DC operating conditions for NMOS and PMOS transistors
- Extended high-voltage modules with ≥ 60V DC operating conditions - NMOS, PMOS and DMOS for 42V board net automotive application
- Triple well isolated CMOS transistors
- Different bipolar transistors
- Double Poly-Si capacitor
- Linear poly capacitor module
- High-resistive Poly-Si resistor
- High precision BSIM3V3 SPICE models for CMOS and Gummel Poon model for bipolars
- Excellent analog performance with accurate device matching
- embedded EEPROM with ready to use EEPROM blocks
- embedded Flash memory with ready to use Flash blocks
- Different digital core cell libraries optimized for speed, low power or low noise
- High density RAM, DPRAM and ROM blocks
- Analog library
- About 2500/4500 effective gates per mm^2 (2ML/3ML)
- 5V and 3.3V I/O cell libraries with CMOS / TTL interfacing capability
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- Optional ESD layer for higher ESD protection
- Development kits for major EDA tools

Applications

- Automotive electronics, communication, industrial and consumer market
- Low-power mixed signal circuits
- High precision mixed signal circuits
- Mixed signal embedded systems; systems on a chip (SOC)
- Analog front ends for sensors
- Circuits with integrated high voltage I/O's and voltage regulators

Quality Assurance

X-FAB spends every possible effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by rigorous quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, VDA 6 and other standards.

Deliverables

- PCM tested wafers
- Optional production services: wafer sort, assembly and final test
- Optional Engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional Design services; e.g. feasibility studies, place & route, synthesis, custom block development

Digital Libraries

- Foundry-specific optimized libraries
- Standard core library for high speed digital blocks
- Low-power library, 50% less power, 40% less area
- Low-noise library with separate bulk contacts for reduced substrate noise
- IEEE 1365 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models
- Synthesis libraries
- Macrofunction and IP's on request
- RAM, DPRAM, ROM
- Zener zaps

Analog Libraries

- Operational Amplifiers
- Comparators
- RC Oscillators
- Bandgaps
- Bias Cells
- Power-On-Reset
- Charge Pumps

Primitive Devices

- NMOS/PMOS Transistors (5V to 60V)
- Bipolar Transistors
- Diodes
- Capacitors
- Poly silicon and diffusion resistors

Ready to use Memory Blocks

- ROM
- RAM
- DPRAM
- EEPROM
- Flash

Process Options

module name	no. of masks	remarks	typical primitive devices applications
CMOS core module	11	5V CMOS core module P-epi wafer, single poly, double metal	5V NMOS/PMOS, analog applications

This main module can be combined with one or more of the following additional modules:

module name	no. of add. masks	remarks	typical primitive devices applications
CAPRES	2	capacitor/ resistor module double poly	double poly capacitor, poly0 resistors (high resistive and/or low TC) for analog applications
LINC *)	1	linear capacitor module linear capacitor implant	linear poly capacitor analog applications
MIDOX	2	mid-oxide module additional thick gate oxide as base for all MV / HV elements	medium voltage NMOS (16V) and high voltage NMOS (60V) analog applications
PMV *)	1	medium voltage p-channel module p-channel MV/HV threshold implant	medium voltage PMOS with or without graded drain (up to 18V) analog applications
NGD *)	1	extended medium voltage n-channel module n-channel graded MV drain implant	medium voltage NMOS with graded drain (21V) analog applications
EEPROM *)	2	EEPROM module EEPROM cell	ready-to-use EEPROM memory blocks, implantation programmed ROM cell, additional capacitors
FLASH *)	3	Flash module Flash cell	ready-to-use Flash memory blocks

Process Options *(continued)*

module name	no. of add. masks	remarks	typical primitive devices applications
PGD *)	1	high voltage graded PMOS module PGD implant	high voltage graded PMOS (33V) additional bipolars, analog applications
HV *)	1	high voltage module high voltage shallow N-well	high voltage PMOS (70V) and extended high voltage NMOS (100V) analog applications
HVE *)	2	extended high voltage module high voltage deep N-well and P-well	extended high voltage DMOS (80V), additional bipolars 42V automotive board net, analog applications
PHVE *)	1	extended high voltage PMOS module specific transistor implant	extended high voltage PMOS (90V) 42V automotive board net, analog applications
ISOMOS **)	4	triple well isolated CMOS module specific transistor implant	low voltage NMOS/ PMOS with isolated bulk, analog applications
METAL3	2	triple metal module additional metal layer	more complex wiring
OPTO	1	optical window module oxide window for photo diodes	optical applications
ESD	1	ESD implant module specific implant for ESD protection	5V ESD-NMOS 5V-I/O's with improved ESD robustness

***) Note:** This module requires the addition of other sub modules as listed in the following table.

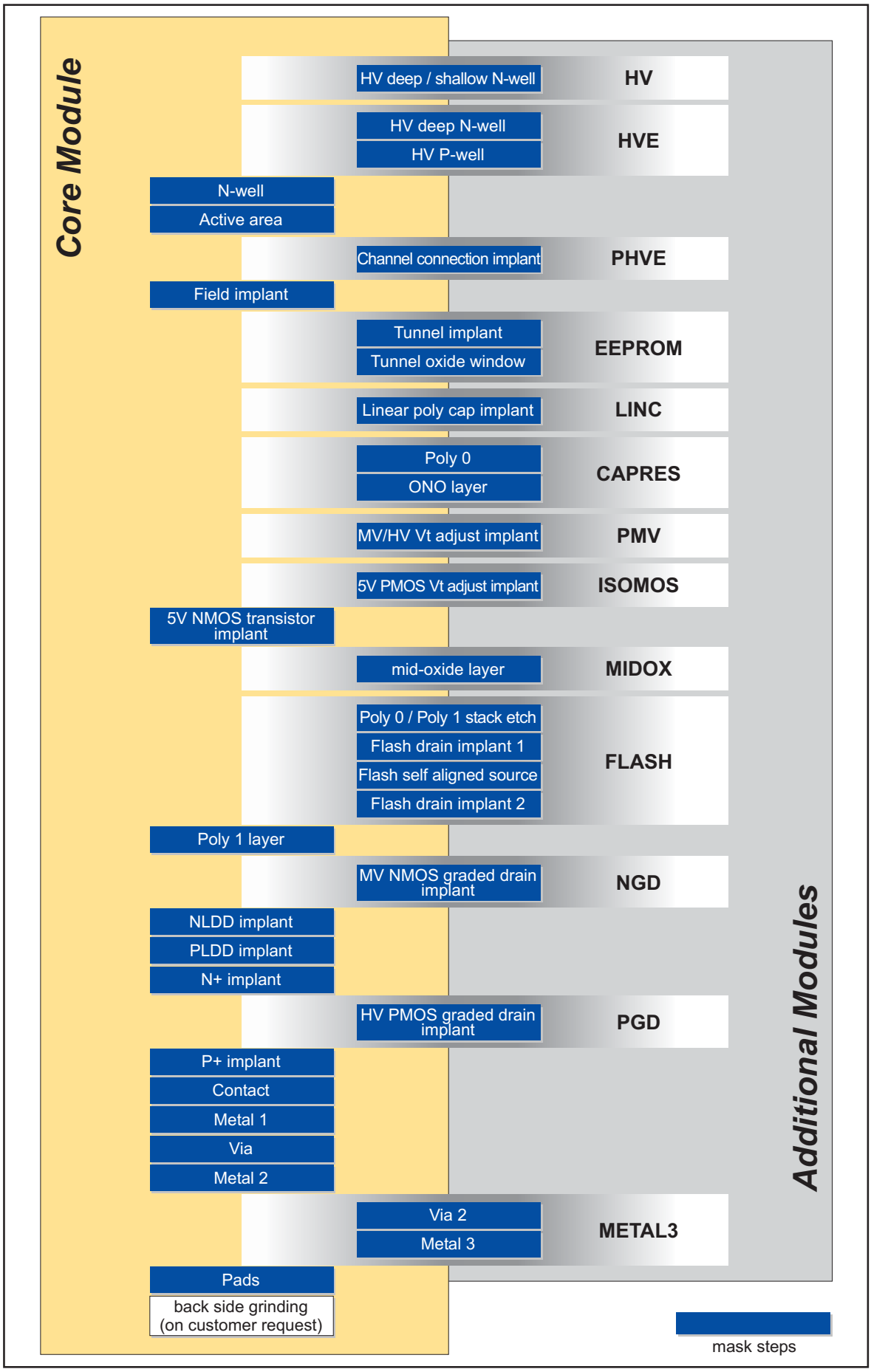
****) Note:** The number of additional masks for this module depends on the combination with other modules (maximum 4, minimum 1).

module name	use of the module also requires the use of following modules
LINC	CAPRES
PMV	MIDOX
NGD	MIDOX
EEPROM	CAPRES, MIDOX, PMV, NGD
FLASH	CAPRES, MIDOX, PMV, NGD, EEPROM
PGD	MIDOX, PMV
HV	MIDOX
HVE	MIDOX. HV
PHVE	MIDOX. HV, HVE

Medium Voltage and High Voltage Modules: Application Recommendations

module name	use of the module also requires the use of following modules
MIDOX	mid-oxide module is the base for all elements with higher than 5V operating voltage it already delivers a 60V NHV transistor
MIDOX+PMV+NGD	are necessary for EEPROM / Flash (switch programming voltages up to 20V)
MIDOX+PMV+PGD	gives possibility for 14V automotive board net because 60V NHV, 33V PGHV and bipolars are available
MIDOX+HV	gives full 14V automotive board net ability with 60V NHV and 70V PHV, additionally already 100V NHVE available
MIDOX+HV+HVE	gives already full 42V automotive board net ability with high and low side switches (NHVE, NDSE)
MIDOX+HV+HVE+PHVE	delivers an additional PHVE for 42V automotive board net
ISOMOS	gives the possibility for triple well isolated low voltage CMOS transistors

Main Process Flow



Schematic Cross Sections

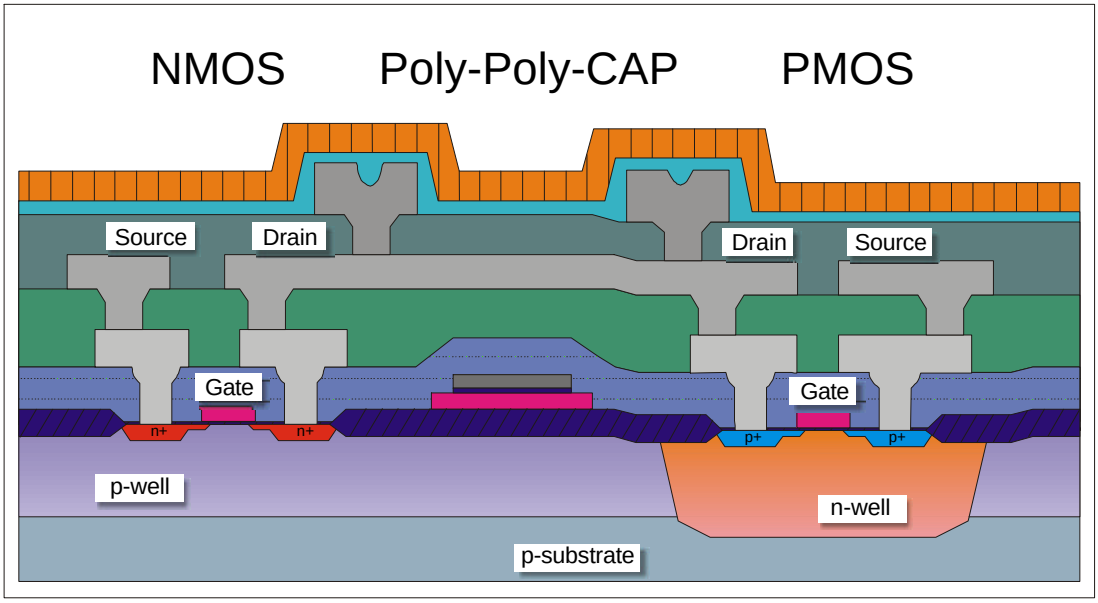


Figure 1: 5V devices

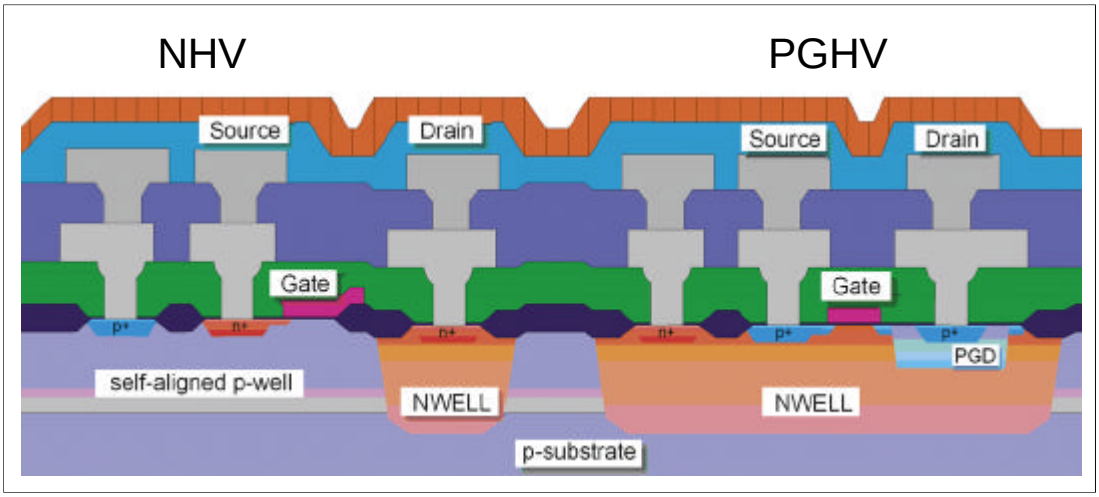


Figure 2: High Voltage devices

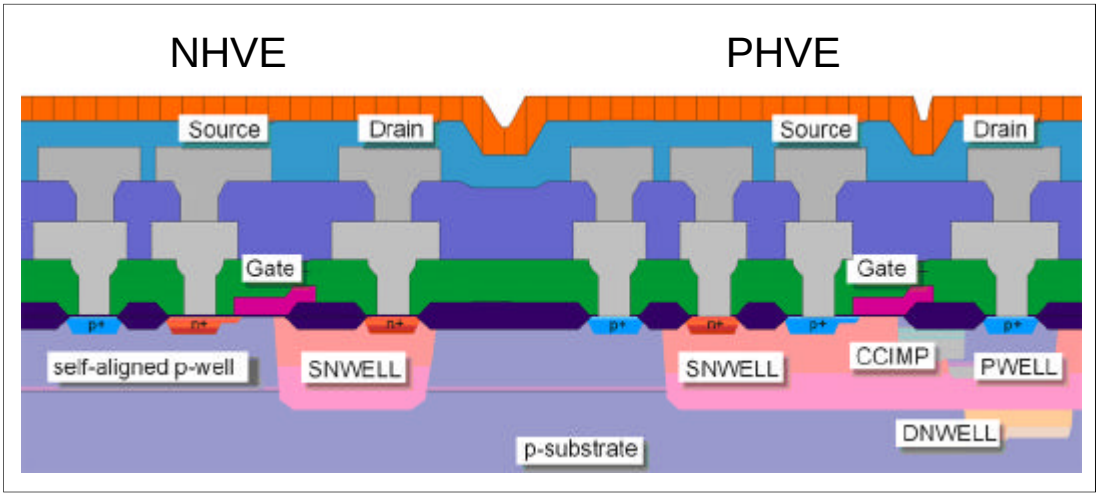


Figure 3: Extended High Voltage devices

Basic Design Rules

Mask	Width [µm]	Spacing [µm]
Standard N-well	4	4.8
HV deep N-well	6	15
Isolated P-well	6	5
Active Area	0.6	1.2
Poly-Silicon Gate	0.6	0.8
Contact	0.6	0.6
Metal 1	0.9	0.8
Via 1	0.7	0.6
Metal 2	0.9	0.8
Via 2	0.7	0.6
Metal 3	1.2	1.0

Device Parameters

The following devices can be used for circuit designs. They are well characterized and part of a primitive device library. The device names correspond with the SPICE model names.

Different reliability tests gave the maximum allowed operating conditions; Values in brackets denote absolute maximum ratings. See also the availability with different options

Active Devices (typical data)

MOS Transistors

Device	Device Name	Avail. only with module	VT [V]	IDS@VGS [µA/µm@V]	|BVDSS| [V]	Max. |VDS| [V]	Max. |VGS| [V]
NMOS 5V	nmos4	CORE	0.83	470@5	13	5.5	5.5
isolated NMOS	nmosi	ISOMOS	0.83	250@3.3	13	3.6	5.5
NMOS medium voltage	nmv	MIDOX	0.9	480@12	16	8	18
NMOS medium voltage low doped drain	ngmv	NGD	0.88	450@12	21	12	18
NMOS high voltage	nhv	MIDOX	0.82	230@12	62	30	18
NMOS extended high voltage	nhve	HV	0.80	205@12	110	60	18
Step-NDMOS extended high voltage	ndse	HVE	0.90	280@12	80	60	18
PMOS 5V	pmos4	CORE	-0.90	220@5	12	5.5	5.5
isolated PMOS	pmosi	ISOMOS	-0.90	100@3.3	12	5.5	5.5
PMOS medium voltage	pmv	PMV	-0.90	180@12	13	8	18
PMOS medium voltage low doped drain	pgmv	PMV	-0.90	150@12	18	12	18
PMOS high voltage graded	pghv	PGD	-0.85	125@12	33	25	18
PMOS high voltage	phv	HV	-0.86	155@12	70	40	18
PMOS extended high voltage	phve	PHVE	-0.93	105@12	100	60	18

Bipolar Transistors

Device	Device Name	Avail. only with module	BETA	VA [V]	|BVCEO| [V]	|Max VCE| [V]
Vertical PNP	qpv5	CORE	12	100	>7	5.57
Vertical HV PNP (collector on bulk)	qpvh	PGD	> 20	> 150	62	40
Vertical ext. HV PNP (collector on bulk)	qpvhe	HVE	70	> 150	80	60
Lateral PNP	qpa	CORE	60	18	>7	5.5
Vertical NPN	qnvo	PGD	60	> 8	> 15	5.5
Vertical ext. HV NPN	qnve	HVE	250	13	>7	5.5

Device Parameters *(continued)*

Passive Devices (typical data)

Capacitors

Device	Device Name	Avail. only with module	Area Cap [fF/µm²]	BV [V]	Voltage Coefficient [%/V]	Temp. Coefficient [10^{-3}/K]	Max VCC [V]
poly1/ metal1/ metal2 cap	csandwt	CORE	0.070				60
poly0/ poly1 cap	cpoly	CAPRES	1.92	20	2.5	0.1	5.5
linear poly0/ poly1 cap	cpolylin	LINC	1.08	30	0.0027	0.04	5.5
deep N-well/poly1/metal1/metal2 cap	csandw	HVE	0.13				60
poly1/metal1/metal2/metal3 cap	csandwtm	METAL3	0.10				60
poly1/ tunnel implant cap	ctm	EEPROM	0.84	40	0.8	0.015	18
poly1/ tunnel implant cap in N-well	ctmw	EEPROM	0.84	40	0.8	0.15	18
tunnel implant/poly0/poly1 cap	ctp0p1	EEPROM	2.61	20	2.5	0.1	5.5

Resistors

Device	Device Name	Avail. only with module	RS [? /✍]	Thickness or junction depth [µm]	Temperature Coefficient [10^{-3}/K]	max VTB [V]
N-well resistor	rnwell3	CORE	900	3.5	6.5	20
poly1 resistor	rpoly1	CORE	17	0.45	1.2	60
N+ resistor in p-substrate	rdiffn3	CORE	55	0.6	1.5	8
P+ resistor in N well	rdiffp3	CORE	110	0.4	1.3	8
low temp. coefficient poly0 resistor	rpoly0	CAPRES	630	0.18	-0.12	60
high resistive poly0 resistor	rpolyh	CAPRES	3500	0.18	-2.5	60
N+ resistor in P well	rdiffnpw3	HVE	55	0.6	1.5	3.6
P+ resistor in deep N well	rdiffpdnw3	HVE	110	0.40	1.3	8
deep N-well resistor	rdnwell3	HVE	625	8	6.3	60
P-well resistor in deep N-well	rpwell3	HVE	6000	1.6	5.8	40
Metal	MET1	CORE	0.08	0.67	3	>60
	MET2	CORE	0.05	1.0 / 0.8	3	>60
	MET3	CORE	0.05	1.0	3	>60

Device Parameters *(continued)*

Misc. Devices

Memory Blocks		
EEPROM		
Ready-to-use EEPROM blocks up to 32 kbit with internal charge pump for programming modes		
Power supply range:	1.8 to 6.0 V	
Current consumption:	< 120 µA (typical)	
Temperature range:	-40 to +125 °C	
Erase / write time:	min. 4 ms	
Number of erase / write cycles	min. 1 x 10^5 @ 25°C	
	min. 1 x 10^4 @ 125°C	
Data retention:	10 years @ 125°C	
Data access time:	< 0.8 µs	
Area (example): embedded block incl. charge pump	256 x 16 bit:	0.60 mm²
	1k x 32 bit:	2.27 mm²
Flash		
Ready-to-use Flash blocks up to 32k x 16 bit (512 kbit) with ECC logic to increase reliability		
Power supply range:	5.0 ± 0.5 V	
External programming voltages:	VPG = 12.0 ± 0.5V	
	VPD = 8.5 ± 0.5V	
	VPS = 12.5 ± 0.5V	
Temperature range:	-40 to +125 °C	
Erase time (flash):	max. 20 pulses with 2ms each, typical 5 pulses	
Write time (per word):	max. 20 pulses with 5µs each, typical 5 pulses	
Number of erase / write cycles:	min. 1x10^3 (-40 to +125 °C)	
Data retention:	10 years @ 85°C	
Data access time:	< 100 ns)	
Embedded block area (examples):	32k x 16 (512kbit):	13.7 mm²
	8k x 16 (128kbit):	4.2 mm²

Note: General characteristics. For detailed values check the datasheet of the available blocks

Digital Core Library Cells

X-FAB provides three different core libraries optimized for most typical applications in mixed signal ASIC.

- The standard core library is optimized for best synthesis results in high speed applications.
- The low power library is designed to achieve best results for low power and small area.
- The third library is a low power library which uses separate bulk contact to reduce the influence of supply switching noise to substrate

Name	Category	Density [1]	@ r_factor [2]	Main features
D_CELLS	standard	ML2: 1.3 ML3: 2.3	ML2: 2.86 ML3: 1.67	**high speed**
D_CELLSL	low power	ML2: 2.5 ML3: 4.5	ML2: 2.86 ML3: 1.67	**min area, min power consumption**
D_CELLSL_B	low power / low noise	ML2: 2.1 ML3: 3.7	ML2: 2.86 ML3: 1.67	**min noise, min power consumption**

1) averaged value: kGE/mm2 (GE = NAND2 Gate Equivalent)
ML2: 2 metal layer routing
ML3: 3 metal layer routing

2) average value: r_factor = Routing_factor
Place&Route_area = Cell_area * Routing_factor

Digital I/O Cells

I/O cells are available for 5 V and 3.3 V operation voltage. Two I/O ring systems are available for pad-limited and core limited designs.

Name	Height	Pad pitch	Main features
IO_CELLS	430µm	110µm	pad limited
IO_CELLS_F	231.3µm	variable	core limited

Input	CMOS	TTL	Pull-up	Pull-down	Output
Standard Input	■	■	■	■	
Schmitt-Trigger	■	■	■	■	
Bi-directional	■	■	■	■	1 - 8 mA (24 mA)
Slew-Rate Control Option	■	■	■	■	4 - 8 mA (24 mA)

Output	1 mA	2 mA	4 mA	8 mA	16 mA	24 mA
Standard	■	■	■	■	■	■
Slew-Rate Control Option			■	■	■	■
3-State	■	■	■	■	■	■
Open Drain	■	■	■	■	■	■

Note: Not all combinations of inputs and outputs are available as bidirectional cell. The core limited I/O library doesn't support the Slew-Rate Control Option.

Analogue Primitive Devices and Models

A very wide range of different analog primitives enable analog designers to develop sophisticated, high precision and reliable analog circuits.

High performance process modules, well defined primitives devices and accurate device models are key success factors for analog and mixed-signal design. Combined with X-FAB's CAE support kit "TheKit" and state of the art design methodologies first right mixed-signal designs are reality.

X-FAB supports BSIM3 models as the present SPICE model standard for MOS transistors. Bipolar transistors are modeled using the Gummel-Poon model. Well resistors have a non-linear terminal-voltage and bulk-voltage dependence. These resistances have to be simulated with the 3-terminal SPICE JFET model.

Model sets for most popular analog simulators, e.g. Spectre, HSPICE, ELDO and PSPICE are provided.

The same characterization and modeling effort is spent for parasitic devices and 3rd order parameters which are usually very important for analog design.

The matching behavior of MOS transistors, bipolar transistors, resistors and capacitors is very intensively investigated and characterized. Final matching parameters are extracted for all active and most of passive elements. These parameters are used at simulator model implementation for Monte Carlo simulation.

Examples for measured and modeled parameter characteristics

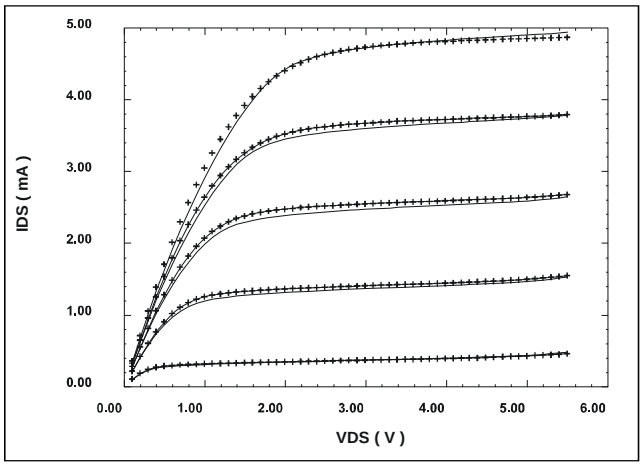


Figure 4:
NMOS4 output characteristic of a typical wafer.
W/L = 10/0.6, VGS = 1.4, 2.3, 3.2, 4.1, 5 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

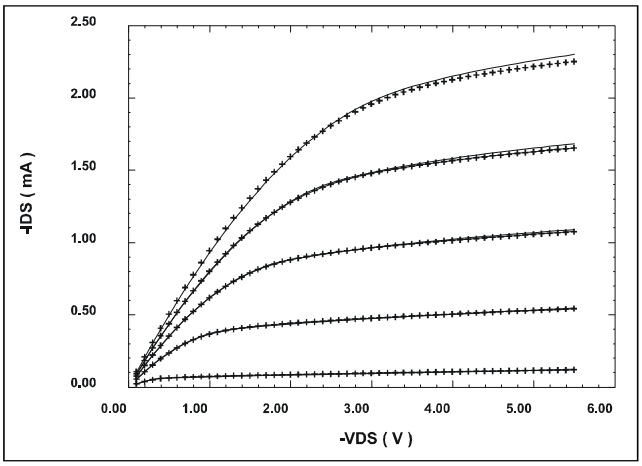


Figure 5:
PMOS4 output characteristic of a typical wafer.
W/L = 10/0.6, -VGS = 1.4 ,2.3 ,3.2 ,4.1, 5 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

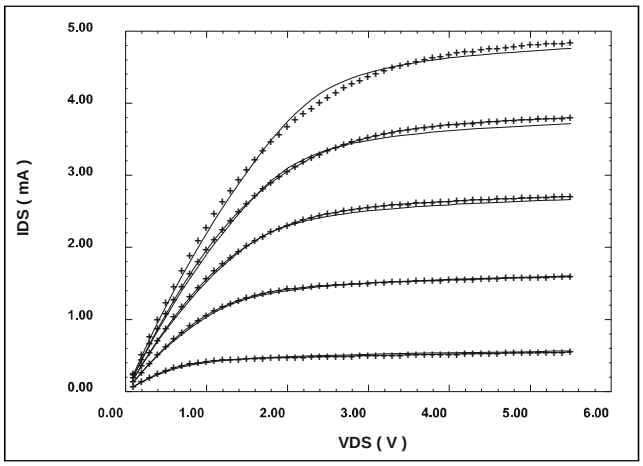


Figure 6:
NMV output characteristic of a typical wafer.
W/L = 10/1.2, VGS = 2.67, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

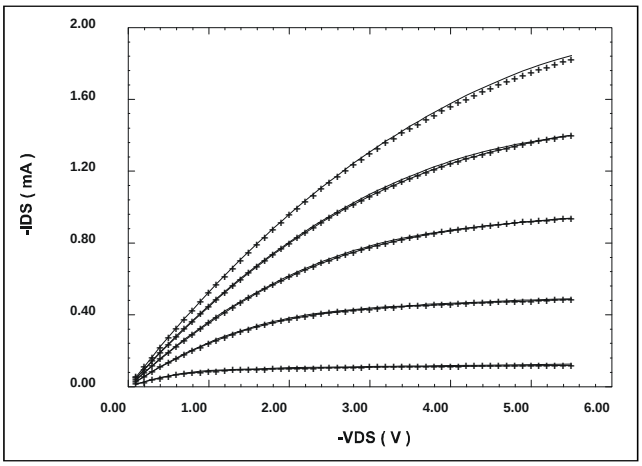


Figure 7:
PMV output characteristic of a typical wafer.
W/L = 10/1.2, -VGS = 2.67, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

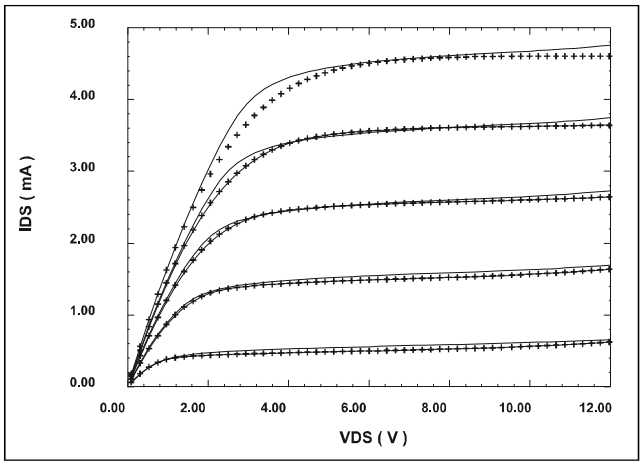


Figure 8:
NGMMV output characteristic of a typical wafer.
W/L = 10/1.4, VGS = 2.67, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

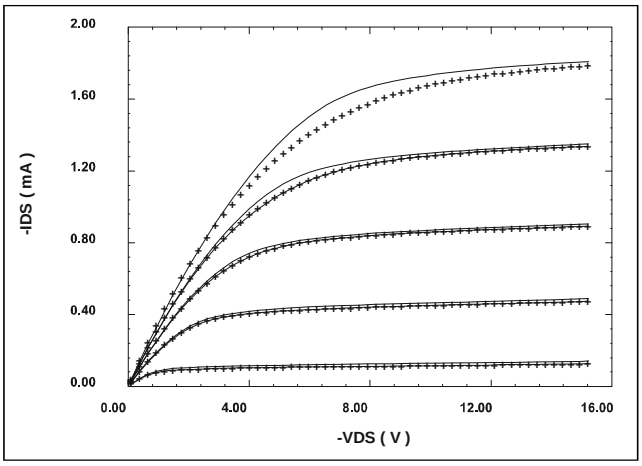


Figure 9:
PGMMV output characteristic of a typical wafer.
W/L = 10/1.2, -VGS = 2.67, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

Examples for measured and modeled parameter characteristics *(continued)*

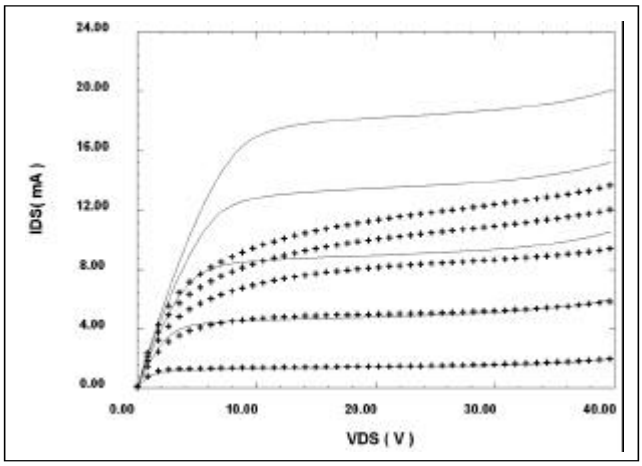


Figure 10:
NHV output characteristic of a typical wafer.
W/L = 50/4, VGS = 2.67, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

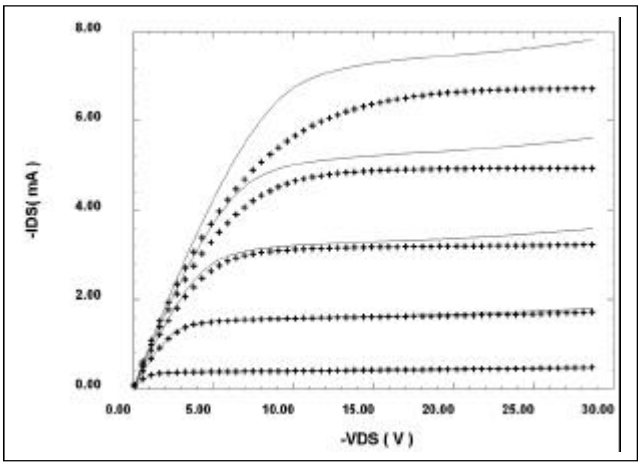


Figure 11:
PGHV output characteristic of a typical wafer.
W/L = 50/5, -VGS = 1.4, 2.3, 3.2, 4.1, 5 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

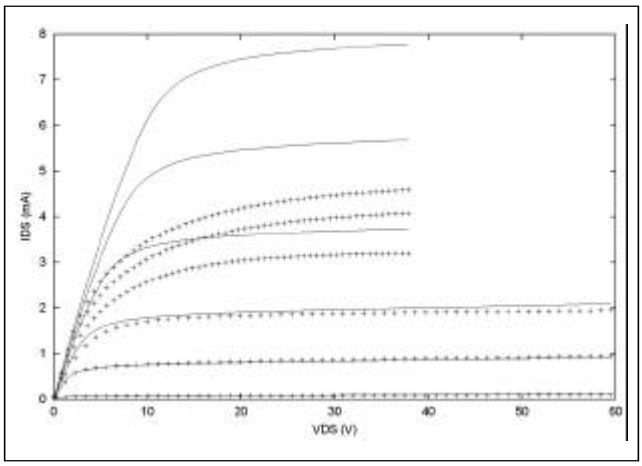


Figure 12:
NHVE output characteristic of a typical wafer.
W/L = 20/3.5, VGS = 1.4, 3.2, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

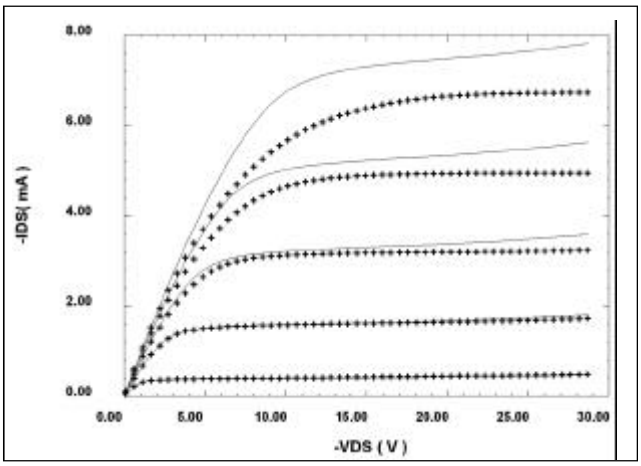


Figure 13:
PHVE output characteristic of a typical wafer.
W/L = 20/4, -VGS = 1.4, 3.2, 5, 7.33, 9.66, 12 V
VSB = 0 V, + = measured, solid line = BSIM3v3 model

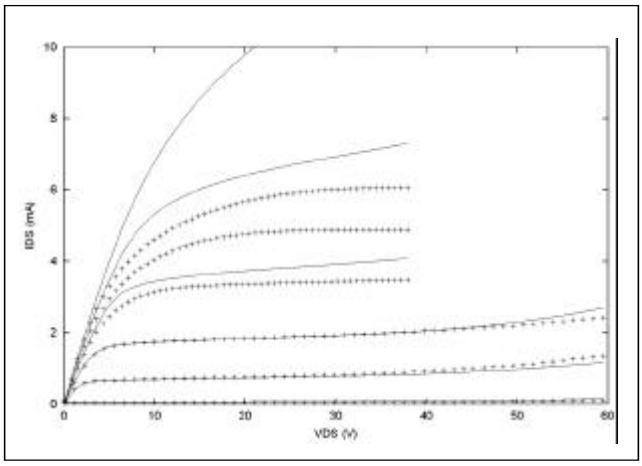


Figure 14:
NDSE output characteristic of a typical wafer.
W/L = 20/2, VGS = 1.4, 3.2, 5, 7.33, 9.66, 12 V, VSB = 0 V,
+ = measured, solid line = BSIM3v3 mode

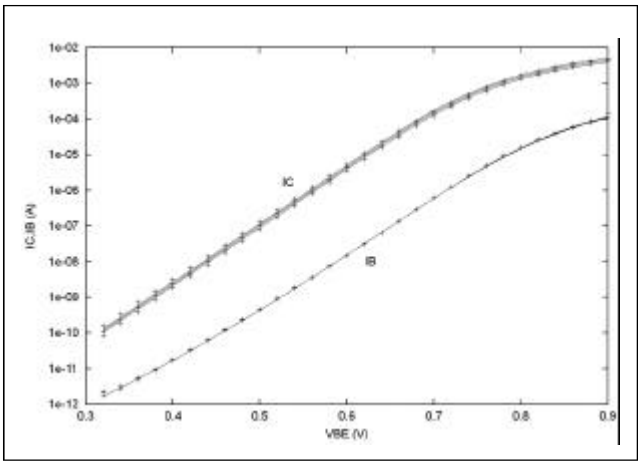


Figure 15:
Gummel plot of vertical NPN bipolar transistor QNVE for a typical wafer.
LE = 20µm, VCE= 1, 3, 5V,
+ = measured, solid line = SPICE model

Examples for measured and modeled parameter characteristics *(continued)*

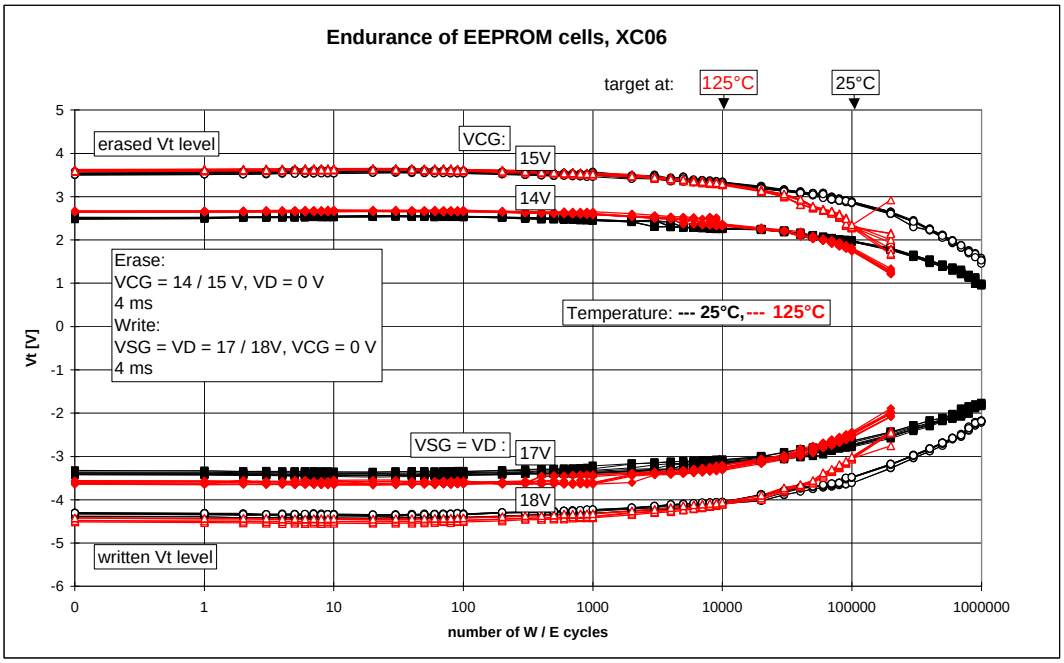


Figure 16:
Endurance of EEPROM cells

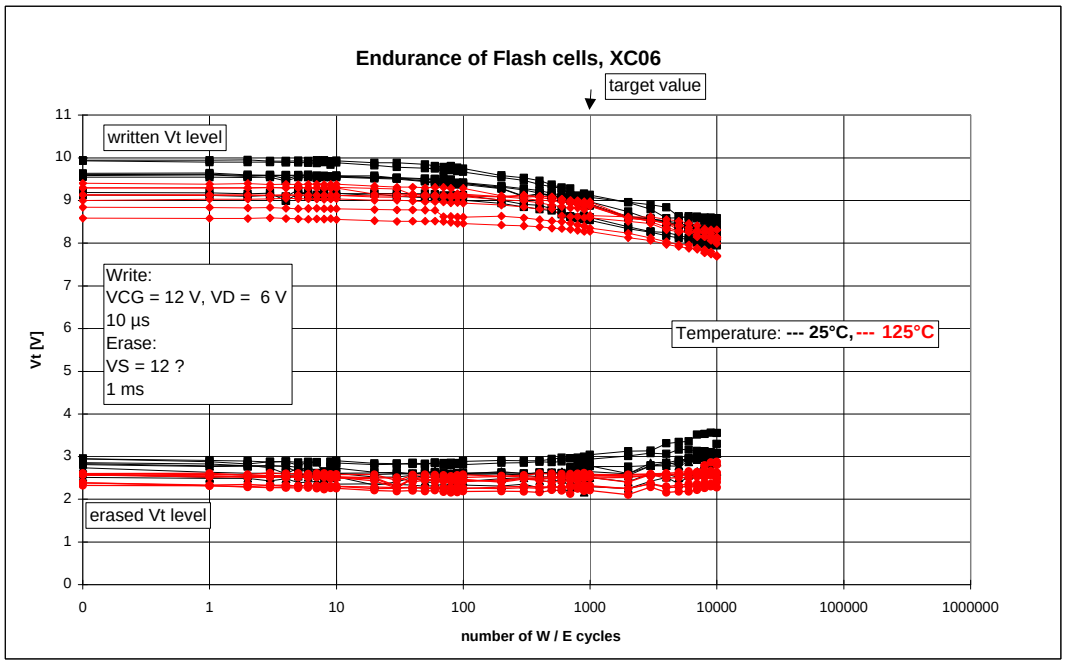


Figure 17:
Endurance of Flash cells

Analogue Library Cells

Many analog and mixed-signal design projects are started in old technologies because designers want to re-use existing analog cells.

For easy migration to X-FAB's high performance XC06 process an increasing number of general purpose analog cells are provided.

Operational Amplifiers

Name	V_{OL} [V]	V_{OH} [V]	V_{ICR} [V]	V_{IO} [mV]	A_{VD} [dB]	B_1 [kHz]	SR [V/µs]	PHM [°]	I_{DD} [µA]	max. Load	Required Module
aopac01	0.02	V_{DD}-1.8	0.1 ... V_{DD}-1.26	<10	107	131	0.1/0.1	60	15	100pF/1000kW	CORE
aopac02	0.05	V_{DD}-0.05	1.28 ... V_{DD}-0.26	<10	96	3350	5.4/5.6	65	530	50pF/50kW	CAPRES
aopac03	0.67	V_{DD}-0.05	1.19 ... V_{DD}-0.19	<10	99	2600	2.0/1.05	60	160	25pF/30kW	CAPRES
aopac06	0.05	V_{DD}-0.05	1.08 ... V_{DD}-0.2	<10	97	3360	2.8/2.7	70	350	50pF/100kW	CAPRES
aopac07	0.05	V_{DD}-0.05	0.12 ... V_{DD}-1.5	<10	99	2680	2.7/2.8	85	210	50pF/100kW	CAPRES
aopac08	0.05	V_{DD}-0.05	1.5 ... V_{DD}-0.2	<10	110	2300	2.0/2.0	70	350	50pF/50kW	CAPRES
aopac09	1.2	V_{DD}-0.6	1.2 ... V_{DD}-0.3	<10	100	7600	6.3/6.4	65	770	100pF/10kW	CORE

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Opamps feature a standby mode

Comparators

Name	V_{ICR} [V]	T_{PD} for 50mV Overdrive [ns] L->H / H->L	T_{PD} for 500mV Overdrive [ns] L->H / H->L	Conditions C_L [pF]; R_L [kW]	Input Offset Voltage [mV]	Supply Current [µA]	Required Process Module
acmpc01	1.0 ... V_{DD}-0.2	670 / 220	-	0.5; 1000	<10	-	CORE
acmpc02	0.1 ... V_{DD}-1.1	630 / 320	-	0.5; 1000	<10	-	CORE

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Comparators feature a standby mode

Bandgaps

Name	Bandgap Voltage (unloaded) [V]; T = 30°C min / typ / max	Temperature Coefficient [ppm/°C]	Supply Current [µA]	Required Process Module
abgpc01	- / 1.281 / -	+200; T= -40 °C to T= 20°C +50; T= 20 °C to T= 85°C	30	CORE
abgpc02	- / 1.211 / -	+100; T= -40 °C to T= 20°C +100; T= 20 °C to T= 85°C	25	CAPRES
abgpc03	- / 1.227 / -	+80; T= -40 °C to T= 20°C +60; T= 20 °C to T= 85°C	57	CAPRES
abgpc04	- / 1.248 / -	+200; T= -40 °C to T= 20°C +100; T= 20 °C to T= 85°C	3.7	CAPRES

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C , all Bandgaps feature a standby mode

Bias Cells

Name	Bias Voltage V_{BP} for PMOS [V]; @V_{DD}=5V, T=30°C	Temperature Coefficient IVBP [ppm /°C]	Bias Voltage V_{BN} for NMOS [V]; @V_{DD}=5V, T=30°C	Temperature Coefficient IVBN [ppm /°C]	Supply Current [µA]	Required Process Module
abiac01	V_{DD}-1.025	-1000	0.964	-1250	6.5	CORE
abiac02	V_{DD}-1.236	-1100	1.29	-1120	12	CORE
abiac03	V_{DD}-1.474	-1150	1.28	-1200	23	CORE
abiac04	V_{DD}-1.027	-3020	0.966	-3000	6.5	CAPRES
abiac05	V_{DD}-1.243	-750	1.133	-750	12.5	CAPRES
abiac06	V_{DD}-1.478	-800	1.295	-850	32	CAPRES

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Bias Cells feature a standby mode

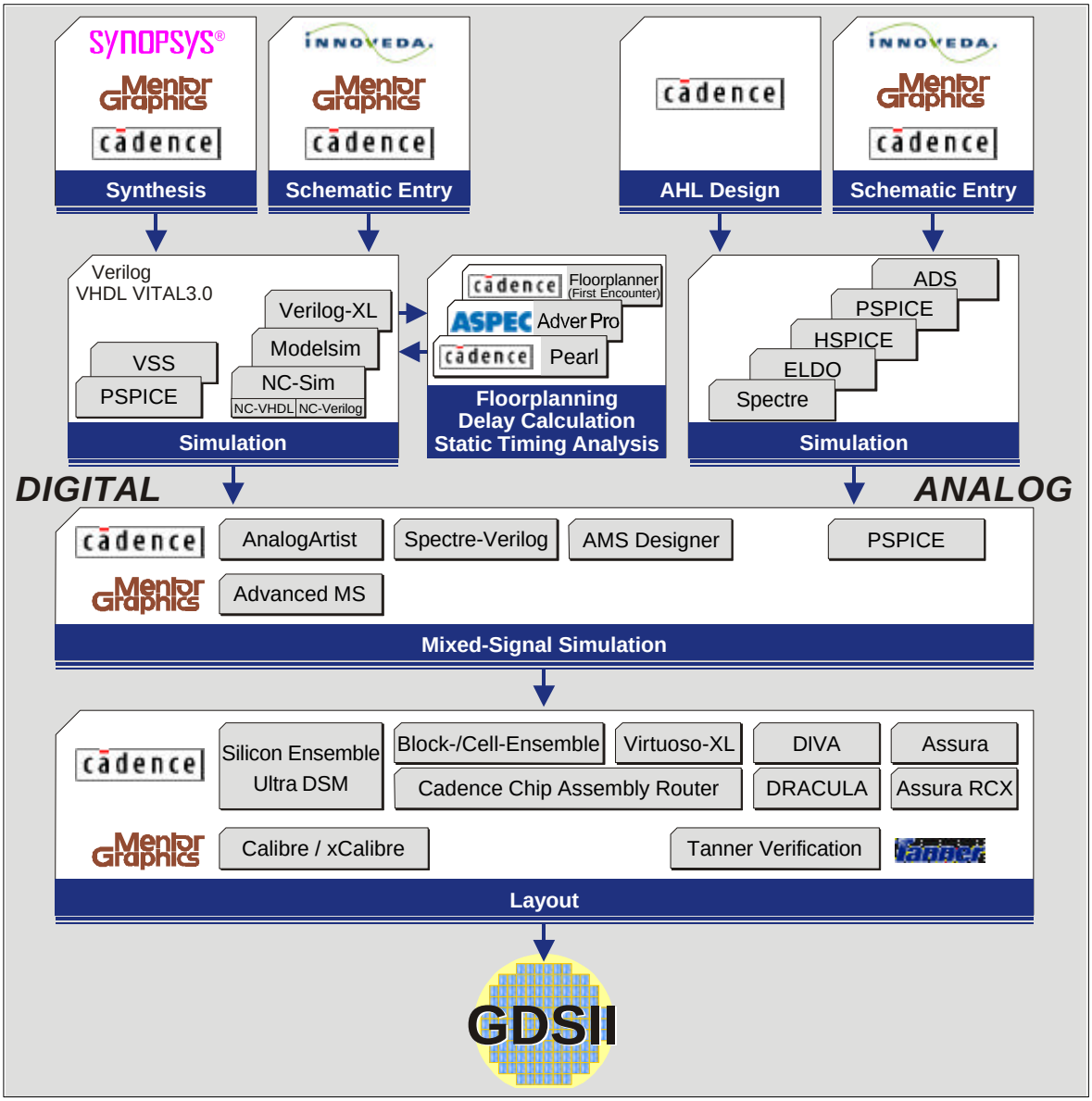
Analogue Library Cells *(continued)*

RC Oscillators				
Name	**Frequency [kHz]**	**Conditions**	**Supply Current (specified @ VDD=5V, T=25°C) [µA]**	**Required Process Module**
arcoc02	133 / 200 / 382	@V_{DD}=5V; T=25°C dig. code= 0h / 10h / 1Fh	73	CAPRES
arcoc03	10	@V_{DD}=5V; T=25°C	3.8	CORE
arcoc04	200	@V_{DD}=5V; T=25°C	73	CAPRES
arcoc05	1000	@V_{DD}=5V; T=25°C	100	CAPRES
arcoc06	670 / 1000 / 1860	@V_{DD}=5V; T=25°C dig. code= 0h / 10h / 1Fh	5	CAPRES
Note: All Parameters are valid for V_{DD}: 4.5 V to 5.5V, T: -40 ....85 °C				

Power-On-Reset				
Name	**High/Low Treshold Voltage [V]**	**T_{DEL} [µs] Delay V_{DD} -> H to POR -> L typical**	**I_{DDL} [µA] DC-Current POR**	**Required Process Module**
aporc01	2.24 / 2.02	3.2	0.01	CORE
aporc02	1.885 / -	5.7	1.8	CORE
aporc03	2.03 / -	5.0	3.2	CORE
Note: All Parameters are valid for V_{DD}: 4.5 V to 5.5V, T: -40 ....85 °C				

Charge Pumps				
Name	**Clock Frequency [MHz] min / typical / max**	**Output Voltage [V]**	**Supply Current [µA]**	**Required Process Module**
achpc01	0.25 / 1.0 / 2.0	6.24; I_{load} = 0 µA 5.68; I_{load} = 10 µA 5.33; I_{load} = 20 µA	12; I_{load} = 0 µA 40; I_{load} = 10 µA 52; I_{load} = 20 µA	CAPRES
Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ....85 °C				

Supported CAE Tools



X-FAB's IC Development Kit "TheKit"

The X-FAB IC Development **Kit** is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard CAE tools and X-FAB's processes and libraries. TheKit is available in two versions, the Master Kit and the Master Kit Plus. Both versions contain documentation, a set of software programs and utilities, digital and I/O libraries which contain full front-end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well.

The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

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